



DESIGN AND ANALYSIS OF LOW POWER HIGH SPEED BODY BIAS CONTROLLED CURRENT LATCH SENSE AMPLIFIER

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Abstract: Sense amplifiers are extensively used in memory. Sense amplifiers are one of the most vital circuits in the periphery of CMOS memories. We know that memory is the heart of all digital systems. Today all worlds are demanding high speed and low power dissipation as well as small area. We know that speed and power dissipation of memory is overall depends upon the sense amplifier we used and their performance strongly affects both memory access time, and overall memory power dissipation. So it is important to design a good sense amplifier which performs well in both speed and power dissipation. In this dissertation, an implementation of a most efficient sense amplifier is done by comparing the best known sense amplifier in today. The dissertation focuses on design, simulation and performance analysis of sense amplifiers.

In this paper, current latch sense amplifier and body bias controlled current latch sense amplifier are designed and results compared. The result shows that the body bias controlled current latch sense amplifier is performing best. The result also shows a novel sense amplifier which consumes small power at same time its speed is faster than other sense amplifiers.

All the designs have been implemented, synthesis and simulated on 180nm CMOS technology using tanner tool version 13.1.

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INTRODUCTION

Digital system design in an amazing and emerging field now days. Each and every digital system has adequate memories. In memory today the CMOS memories are used in a much greater quantity than all the other types of semiconductor integrated circuit. SRAMs are used as large caches in microprocessor cores and serve as storage in various inputs on a system-on-chip like graphics, audio, video and image processors. SRAMs also used in high performance microprocessors and graphics chips so for each generation to bridge the increasing divergence in the speeds of the processor and the main memory we need high speed requirements. At the same time, SRAMs used in application processors which go into mobile, handheld and consumer devices have very low power requirements. So power dissipation has become an important consideration both due to the increased integration and operating speeds, as well as due to the explosive growth of battery operated appliances. As with other integrated circuits today, CMOS memories are required to increase speed, improve capacity and maintain low power dissipation.

To read the contents of this memory a sense amplifier is used. The sense amplifier converts the arbitrary logic levels of bitlines to the digital logic levels which required running the peripheral Boolean circuits of outside world of memory. In the SRAM data path, switching of the bitlines, I/O lines and biasing the sense amplifiers consume a significant fraction of the total power. Mainly performance of memory depends on the performance of SA such as delay and power dissipation.

So the sense amplifier is one of the most circuits in the periphery of CMOS memories. Speed and power dissipation of the memory is mainly depends on types of sense amplifier used. So performance of SA strongly affects both memory access time, and overall memory power dissipation.

Power dissipation was not the main issue' just proper output and the circuit operation was the main preference. The low power intend in circuit design is used because of:

1. If the system dissipates high power, then extra design is required for the cooling system, thus the system will become very bulky and will not be portable
2. Due to the extra cooling system the cost of the system will increase.
3. Due to the sky-scraping power dissipation the performance and reliability of the system decreases



4. Memory is the main and important field of design. Today the size of the memory is decreasing and the storing capacity is increasing. As the storing capability is increasing, the time response for the data writing and reading from the memory should be very fast. For this purpose different types of sense amplifiers are used.

NECESSITY OF SENSE AMPLIFIER

In the memory, it is common to reduce the voltage swing on the bit lines to a value significantly below the supply voltage. This reduces both the propagation delay and the power consumption. Noise and other disturbances may be occurred in the memory array for this sufficient noise margin is obtained even for these small signal swings. During the interfacing of the memory to the external field, the amplification of the internal swing is required. This is achieved by the sense amplifiers. Design of a high performance and efficient sense amplifier is very important for design SRAMS but with increasing parameter variations, the developing of a reliable and fast sense amplifier is a big problem in itself. Sense amplifiers play a major role in the functionality, performance and reliability of memory circuit. Reduction in delay and power is acquired by using sense amplifier in memory circuits.

The designed sense amplifier should be standard and capable to support the current SRAM design without significantly affecting the other devices of peripherals of SRAM.

BASIC OF SENSE AMPLIFIER

A sense amplifier is an active analog circuit that reduces the time of signal propagation from an accessed memory cell to the logic circuit located at the periphery of the memory cell array, and used to detect small variation on bitlines of memory and produce full voltage swing it means that converts the arbitrary logic levels occurring on a bitline to the digital logic levels of the peripheral Boolean circuits. The sense amplifier circuit has to operate within the conditions which are set by the operation margins. Operation margins in a digital circuit are those domains of voltages, current and charges. These domains unambiguously represent data throughout the entire operation range of the circuit. Operation margin depends on the circuit design, processing technology and environmental conditions. Sense amplifiers, used with memory cells, are key elements in defining the performance and environmental tolerance of CMOS memories. Because of their great importance in memory

designs, sense amplifiers became a very large circuit-class. CMOS memories are used in a much greater quantity than all the other types of semiconductor integrated circuits, and appear in an amazing variety of circuit organizations.

Memory Sensing and amplifying the information signal which transfers over memory cell to bit lines are the most important ability for a sense amplifier. However, to sense the data correct and fast turn into more and more difficult when the operational voltage scales down to low voltage. In an integrated circuit "sensing" means the recognition and resolve of the data content of a selected memory cell. The sensing may be "nondestructive," when the information content of the selected memory cell is unaffected (e.g., in SRAMs, ROMs, PROMS, etc.), and "destructive," when the information content of the selected memory cell may be altered (e.g., in DRAMS, etc.) by the sense operation. Sensing is performed in a sense circuit.

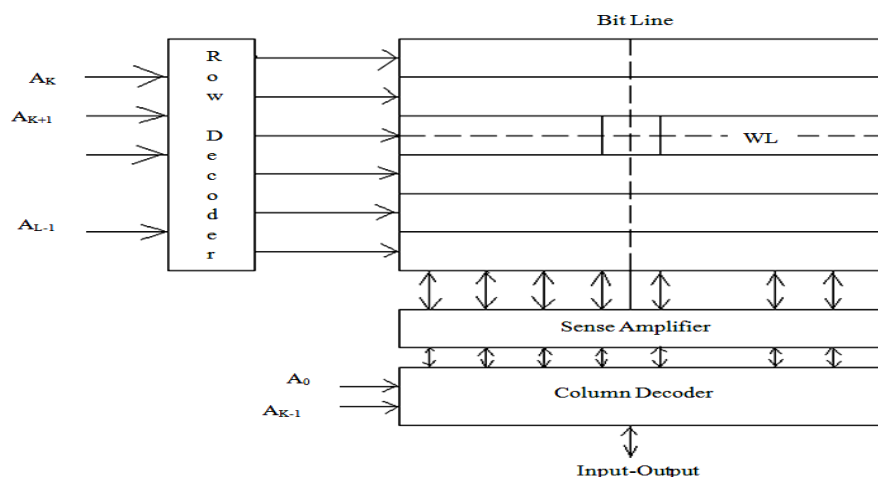


Fig. 1 Memory Architecture

DESIGN IMPLEMENTATION AND SIMULATION OF SENSE AMPLIFIERS

On the modern trends quick memories are highly required with low power consumption. The low power and low voltage CMOS techniques were applied extensively in analog and mixed mode circuits for the compatibility with the present IC technologies. Low power consumption can be achieved by using sense amplifiers which are main part of CMOS memory. Parasitic capacitance is much higher if memory is of high density. The large capacitance is an issue to make our each cell more energy to charge means low to sense amplifier. To achieve a faster memory and less power dissipation we have to design sense amplifiers as. Increase in number of cells per bit line which will increase the parasitic capacitance. Minimize supply voltage lead to short noise margin that affects the sense



amplifier reliability. To maintain small voltage swing over the bit line, increase the area of each cell for design more memory on the chip which decreased the load on bit line. The wide range of applications of sense amplifier as it provides a photovoltaic system which usually stores enough energy for uncertainty in availability of solar radiation due statically nature of biosphere. These typical ICs are the complex component to measure the charge battery and discharge current. sense amplifiers plays a very smart role to maintain the reliability , accuracy and extended battery life by cutting power down over certain region to control heat. Mainly two types of SRAM sense amplifier linear amplifier and latch type amplifier.

As previously discussed in chapters about various sense amplifiers, it is found that some sense amplifier consume less power but with more delay than other consume slightly more power but speed (with less delay) is relatively large. In this dissertation I propose a new sensing scheme which has less delay, more sensitivity than previously discussed with less power consumption. This chapter divided into four parts.

- Current latch sense amplifier
- Latch operation
- The Sizing Consideration
- Body-biased controlled Current latch sense amplifier

These sense amplifiers made using with the help of Tanner tool V13.1.

CURRENT LATCH SENSE AMPLIFIER (CLSA)

Latch-type sense amplifiers, or sense amplifier based flip-flops, are very effective comparators. They achieve fast decisions due to a strong positive feedback and their differential input enables a low offset. The sense amplifiers circuit is the heart of memory. The sense amplifiers are mainly designed to read the memory contents and amplify them to proper level using at logic circuits around memory. Sense amplifiers (SA) are hence widely applied in, for example, memories, A/D converters, data receivers and lately also in on-chip transceivers have become especially popular because of their high input impedance, full-swing output and absence of static power consumption. A good SA has the following properties namely, minimum sense delay, minimum power consumption, proper gain for amplification, minimum layout area, highly reliable, less number of cascading of transistors from source voltage to ground for low voltage operation and tolerable to environment. This

kind of sense amplifier circuit is designed for increased speed, sensitivity with reduced power consumption. This design combines aspects from the latch based voltage mode sense amplifier and the differential

Current Latch Sense Amplifier is based on voltage mode sense amplifier. It is also classified in differential type voltage sense amplifier. In this amplifier two cross-coupled inverters are used which give positive feedback as in latch type sense amplifier. But here the bitline is isolated from its output by using extra two nMOS transistors. So it has very high input impedance. The CLSA is shown in Fig 2

CIRCUIT CONFIGURATION

It consists of 5 nMOS and 4pMOS transistors namely MN1, MN2, MN3, MN4, and MN5.

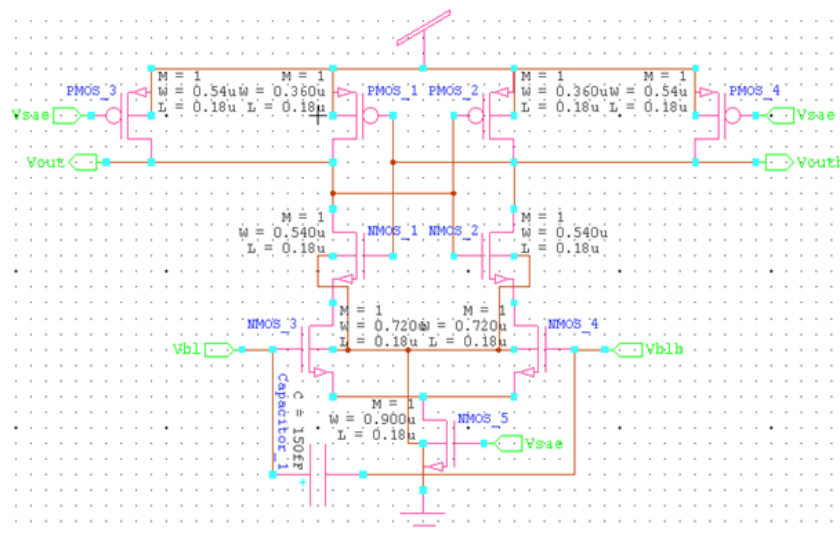


Fig. 2 Current Latch Sense Amplifier (CLSA)

MN1, MP1, MN2 and MP2 make two inverters connected in cross coupled manner give positive feedback in circuit. MN3 and MN4 are used to couple bitlines to CLSA amplifier. MP3 and MP4 are precharge transistors. The capacitor C represents the column capacitance of bitlines for filling of SRAM in circuit. The sense amplifier has following ports namely Vsaee, vout, voutb, bl, blb. The bl and blb are column bit lines of SRAM. The signals are given to the Vsaee which control the precharge and enable CLSA. The amplified output is taken from Vout node and complimentary output at Voutb node.

WORKING OF CURRENT LATCH SENSE AMPLIFIER (CLSA)

The sense amplifier is pre-charged in other words it is reset before sensing the bitlines. This action clears the previously latched data and charged the output nodes to the supply voltage.



When the control signal V_{sae} , is at 0 logic means (low voltage) the pre-charge transistors MP3 and MP4 turned on so the output nodes are charged to supply voltage V_{DD} . When the sense amplifier enable signal V_{sae} is at high, the precharged transistors MP3 and MP4 turned off. But at this time transistors MN5 turned on so the drain of MN5 is pulled down to ground level. Due to this now, transistors MN3 and MN4 are working as a common source differential amplifier.

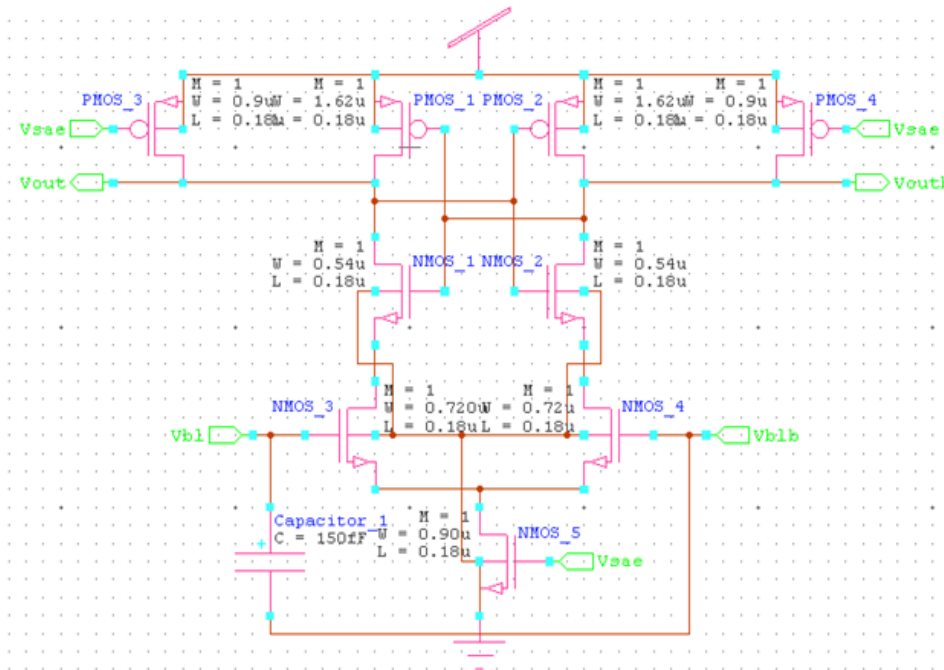


Fig. 3 Current Latch Sense Amplifier (CLSA) with different W/L ratio

Due to the voltage difference developed by bit lines, bl and blb is transferred to drain nodes of transistors by the common source differential amplifier. At this time V_{out} and V_{outb} starts discharging suppose bl at V_{DD} and blb at $V_{DD}-\Delta V$ volts. This result gives more current flow thru MN3 than MN4. Due to this V_{out} node discharged rapidly than V_{outb} . Because out node rapidly discharging, when it reach at enough low level of voltage at this time the MN2 starts to on state. So the very high positive feedbacks loop work very inventively. This action causes $outb$ node charged to V_{DD} level and out node to ground GND. Here transistor MN5 works as current source and transistor MN1, MP1, MN2 and MP2 work as latch and produce very high gain due to positive feedback. The speed of sense amplifier is depends on the how fast output nodes get charged thru pre-charging transistors. So by proper design pre-charge time kept as small as possible. CLSA performed sensing and amplification using without any current from bitlines to outputs so the sense and pre-charge power dissipation can be



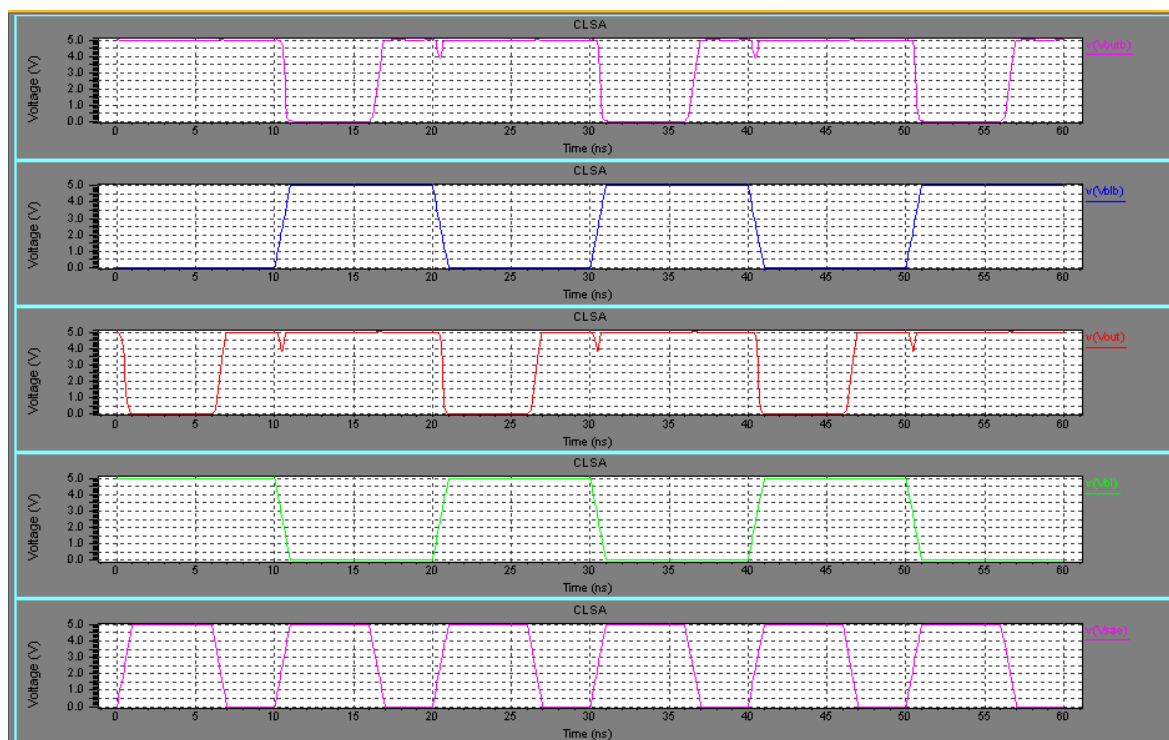
reduced. The main drawback is that it use 4 stages of transistor cascaded from V_{DD} to GND. It give results that CLSA not work at very low voltage due to very low differential current so speed is slow at low V_{DD} .

RESULT ANALYSIS AND COMPARISON

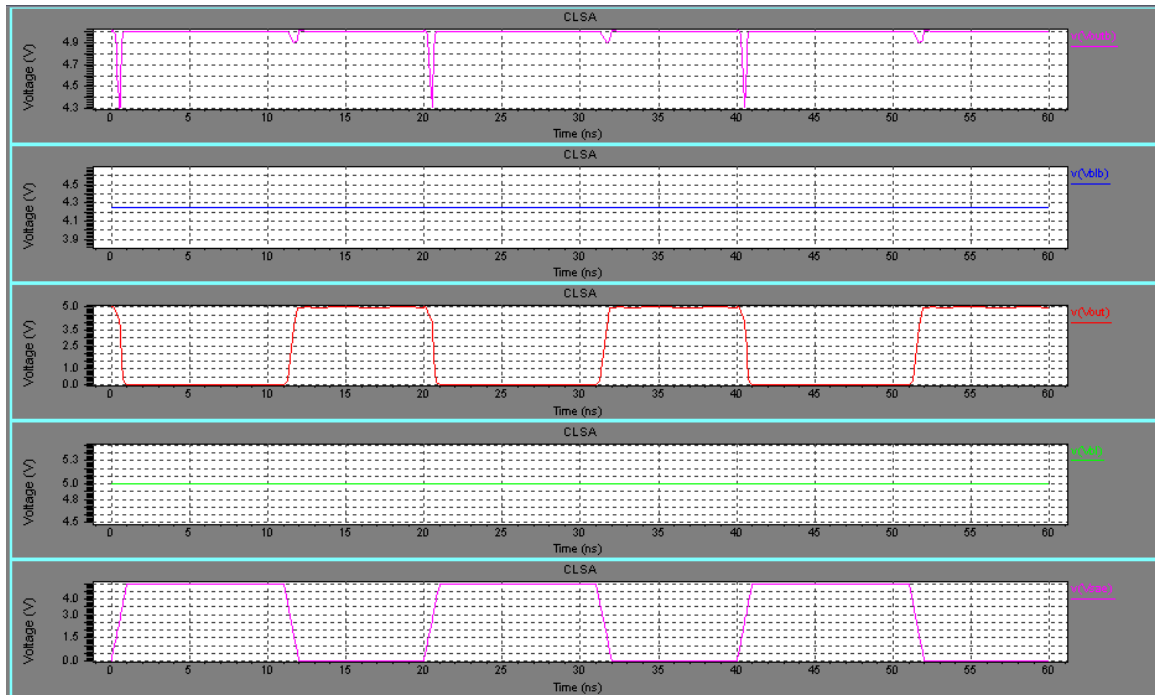
In this chapter here we show that the Simulation results of all implemented sense amplifiers. Function of designs is verified by using simulated based verification. This verification ensures that the design is functionally correct when tested with given set of inputs. Designed sense amplifiers have been implemented and simulated on Tanner tool in 180nm technology.

Current Latch Sense Amplifier (CLSA)

In this section I show the simulation results of Current Latch Sense Amplifier (CLSA). The simulation time is taken for CLSA amplifier is 60 neno seconds. The simulation waveform of the CLSA is shown in figure 5.1. Figure 5.1(a) shows the simulation waveform of the CLSA at $V_{DD}=5$ Volt. V_{sae} given in pulses of 0.5 duty cycle with time period of 10n seconds both rise and fall time is 1n seconds. Similarly bit input to V_{bl} is in bit form and in sequence of 10101 and inverse of this is V_{blb} .The total simulation time is 60n seconds.



(a)



(b)

Fig.4 Simulation waveforms of the Current Latch Sense Amplifier (CLSA) (a) for Bit Voltage (b) For Constant Voltage Difference

Similarly figure 5.1(b) shows the wave form at VDD at 5 volts, Vbl at 5 volts and Vblb taken at 4.25 volts. The functionally this is shown in waveform that when Vsae is at low volts seen in v (Vase), the amplifier pre-charged to VDD. When Vsae is at high level then sense amplifier is in sensing mode so Vout should be 0volt if Vbl is at 5volt otherwise if Vblb is at 5 volts its value at full swing value which is 5volts. We obtained reverse value for Voutb node which is shown as Voutb value.

Table 1 CLSA operation

Vsae	Vbl	Vblb	Vout	Voutb	Remark
5V	5V	4.5 V	0V	5V	In sense mode
0V	5V	4.5 V	5V	5V	In pre-charge mode
5V	4.5V	5 V	5V	0V	In sense mode
0V	4.5V	5 V	5V	5V	In pre-charge mode

This is also true for pulse inputs.

Power dissipation of CLSA

The figure 4 shows the power dissipated by the Current Latch Sense Amplifier at VDD equal to 3V. This dissipation is measured for 100n seconds.

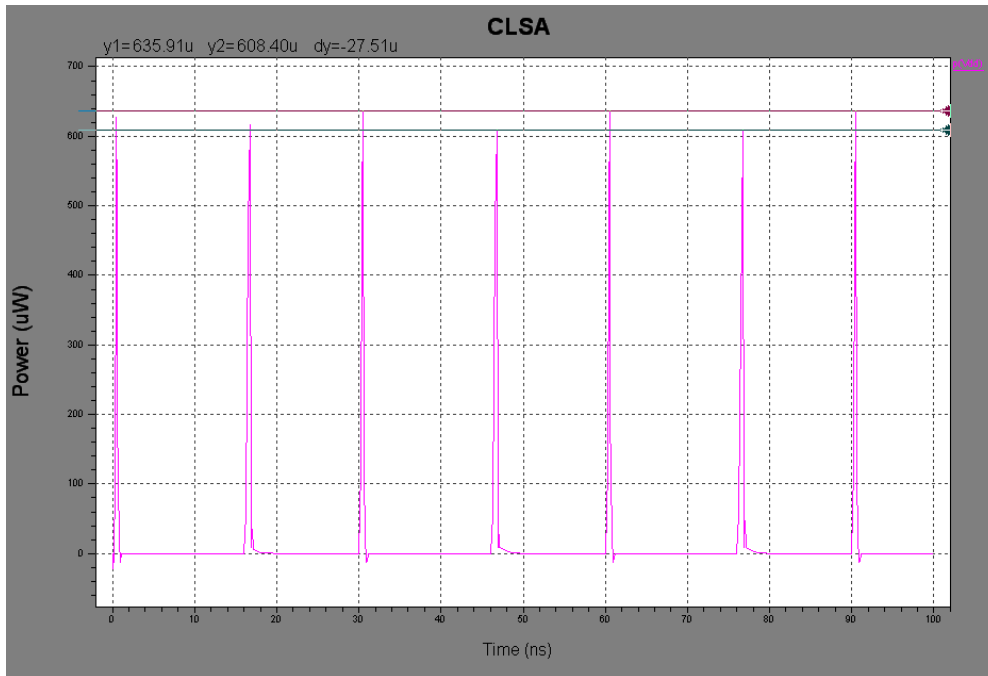


Fig. Simulation waveform of power dissipation of CLSA

Table 2 V_{DD} versus Pre-Charge Delay, Power Dissipation and Noise Margin of BB-CLSA

V_{DD} (V)	Pre-Charge Delay (ps)	Power Dissipation (μW)	Noise Margin V_{IL} (V)	Noise Margin V_{IH} (V)
5V	179	120.505	1.825	2.64
4 V	211.13	74.045	1.315	2.06
3 V	221.98	28.13	0.680	1.51
2 V	241.04	12.695	0.605	1.055
1 V	467.59	5.25	0.436	0.628

CONCLUSION AND FUTURE SCOPE

Conclusion

In this dissertation Body Bias Controlled Current Latch Sense Amplifier has been designed and simulated using 180nm CMOS technology of tanner tool at a various supply voltage from 1.0V to 5.0V. A Sense Amplifier is specially proposed in this dissertation as it is the heart of the Memory. Especially I proposed a BB-CLSA for low power and high speed operations in SRAM. This proposed Sense amplifier is compared with nearest basic Current Latch Sense amplifier as

- The power consumption of proposed BB-CLSA has been reduced from 47% to 87% compared to conventional CLSA.



- Speed of proposed Sense amplifier is increased by 10% as compared to conventional CLSA.
- Noise Margin and Sensitivity of proposed sense amplifier is improved considerably.
- Body Bias method is used for high speed at low power dissipation operation.
- Only 44% more transistors are used to reduce about 87% power dissipation and to get 10% more high speed operation.

Future Scope

However some aspects of the goal have been achieved using this design, but still a better Sense Amplifier can be build by some improvement in the circuit design. The SA can be further extended and modified by the following points.

- Delay can be further reduced by improving circuit design.
- Affect of process variations and corner variations on the performance of the proposed sense amplifiers are not included. So effects of these variations are removed by proper design of circuits and accurate simulations.
- Yield measurements can be done
- The layout can also be designed using L-Edit of tanner tool by which area can be calculated for chip fabrication.
- Body Bias Voltage Latch Sense amplifier is designed for high speed operation.
- In this design we use 180 nm technologies but latest technology 28nm and more can be used for batter design and analysis.
- The layout can also be designed using L-Edit of tanner tool by which area can be calculated for chip fabrication
- The delay and power dissipation can also reduced by using low power and high speed techniques like VTCMOS, DTCMOS, and Adaptive CMOS and Adiabatic logic technology.

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