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# CASCADED H-BRIDGE MULTILEVEL INVERTER USING SPWM

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**Abstract:** *This paper presents the concert of flying capacitor multilevel inverter and cascaded H-bridge multilevel inverter. To improve the performance of Flying Capacitor Multilevel Inverter (FCMLI) the switching pattern selection scheme is used. By this scheme the capacitor voltage fluctuation is reduced without using voltage feedback. The elimination of harmonics in a cascaded multilevel inverter (MLI) by taking the unequal of separated DC source is presented. DC sources may be batteries, solar cells, etc. A fundamental switching scheme is used, which achieves the fundamental in the output voltage while eliminating the lower order harmonics and to produce a nearly sinusoidal output. The FFT spectrums for the outputs are presented to study the reduction in the harmonics. The circuit is simulated using MATLAB/SIMULINK. The simulation results are verified.*

***Keywords***: *Embedded Controller, MATLAB/SIMULINK, H-bridge Multilevel Inverter, THD, Unequal Voltage Sources.*

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## I. INTRODUCTION

Multilevel inverters have very important development for high power medium voltage AC drives. Quite a lot of topologies have found industrial approval;

a. Neutral Point Clamped Multilevel Inverter.
b. Flying capacitor Multilevel Inverter.
c. Cascaded Multilevel Inverter.

Maynard and Foch introduced a flying-capacitor-based inverter in 1992. The structure of this inverter is similar to that of the diode-clamped inverter except that instead of using clamping diodes, the inverter uses capacitors in their place. The cascaded multilevel inverters offer more than two voltage levels. A desired output voltage waveform can be synthesized from the multiple voltage levels with less distortion, at low switching frequency, higher efficiency, and lower voltage rating devices. An important question in designing an effective multilevel inverter is to ensure that, the total harmonic distortion (THD) in the output voltage waveform is small. A complete solution is obtainable for computing all possible switching angles that achieve the required fundamental voltages and eliminate the lower order harmonics [1]. On the other hand, it was assumed that the dc sources were all equal, which will probably not be the case in applications even if the sources are nominally unequal. Here, it is shown how the method in [2] can be extended to two unequal dc source inverter. Particularly, eliminating harmonics in a multilevel converter in which the separate dc sources do not have equal voltage levels is measured. Normally each phase of a cascaded multilevel converter requires n DC sources for 2n + 1 level. For many applications, to get several separate DC sources is difficult, and too many DC sources will be necessary many long cables and might lead to voltage unbalance among the DC sources. To reduce the number of DC sources necessary while the cascaded H-bridge multilevel converter is applied to a motor drive, a scheme is proposed in [3] that allow the use of two unequal DC sources to generate five level equal step multilevel inverter output. In this paper, the lower order harmonics are eliminated using two unequal DC voltages for H-bridges.

## II. FLYING CAPACITOR MULTILEVEL INVERTER

Fig. 1 shows a FCMLI, in this type of inverter uses a ladder structure of dc side capacitors where the voltage on each capacitor differs from that of the next capacitor. n-1 capacitors in

the dc bus are needed to generate n-level staircase output voltage. Every phase-leg has an indistinguishable structure. The size of the voltage increment between two capacitors decides the size of the voltage levels in the output waveform of the inverter.

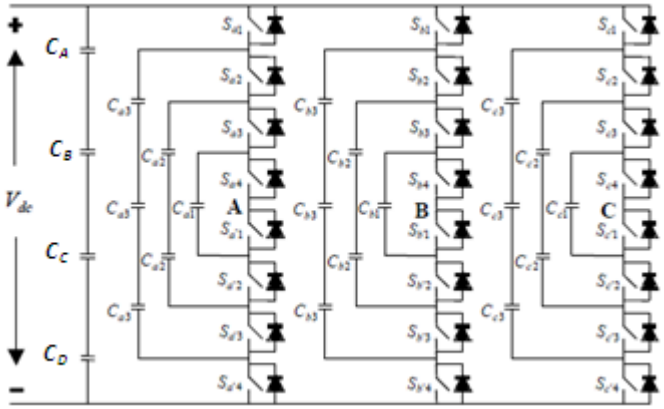


Fig. 1 Three phase flying capacitor multilevel inverter.

It is clear that three inner-loop balancing capacitors for phase leg A, $C_{a1}$, $C_{a2}$, and $C_{a3}$ are independent from those for phase leg B. Every phase legs segregate the same dc link capacitors, $C_A$ to $C_D$. Table I shows the possible switch combinations to generate the five level output waveform.

The voltage synthesis in a five-level flying capacitor converter has more flexibility than a diode-clamped converter [4]. The voltage of the five-level phase-leg A output with respect to the neutral point o, $V_{Ao}$, can be synthesized by the different switch combinations.

TABLE I

SWITCHING STATES OF FIVE LEVEL MULTILEVELINVERTER

| Output Voltage $V_{AO}$ | Switching States Of MLI | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | $S_{a1}$ | $S_{a1}$ | $S_{am-1}$ | $S_{am}$ | $S_{a'1}$ | $S_{a'2}$ | $S_{a'm-1}$ | $S_{a'm}$ |
| $V_5=V_{dc}$ | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| $V_4=3V_{dc}/4$ | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| $V_3=V_{dc}/2$ | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| $V_2=V_{dc}/4$ | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| $V_1=0$ | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

## III. CASCADED H-BRIDGE MULTILEVEL

### INVERTER

The cascaded multilevel inverter consists of a series of H-bridge inverter. The general purpose of this multilevel inverter is to synthesize a desired voltage from several separate

dc sources, like batteries, fuel cells, solar cells, and ultra capacitors. Fig. 2 shows a single-phase structure of a cascade inverter with separate dc sources [5]. Each separate dc source is connected to a single-phase full-bridge inverter.

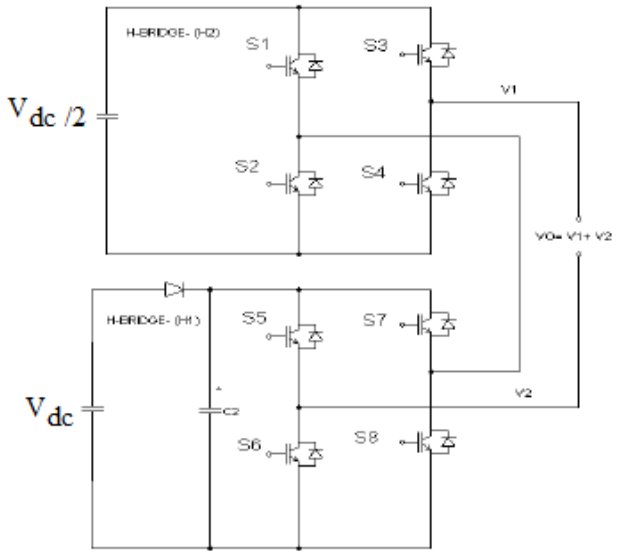


Fig. 2 Topology of a five level H-bridge cascaded multilevel inverter.

The topology offered in this paper employs two unequal dc sources to generate an equal step five level output. The proposed inverter consists of two H-bridges as shown in Fig.2. The main H - bridge ($H_1$) is connected to a dc source of $V_{dc}$ and the second bridge ($H_2$) is connected to a dc source of $0.5V_{dc}$. By suitably opening and closing the switches of $H_1$, the output voltage $v_1$ can be made equal to $-V_{dc}$, 0, or $+V_{dc}$ similarly the output voltage of $H_2$ can be made equal to $-0.5V_{dc}$, 0, or $0.5V_{dc}$ and the cascaded output is shown in Fig.3. Therefore, the output voltage of the converter can have five possible values $V_{dc}$, $0.5V_{dc}$, 0, $-0.5V_{dc}$, and $-V_{dc}$

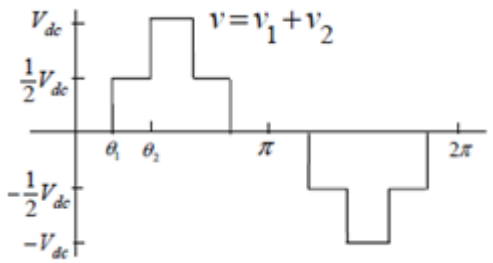


Fig. 3 Fundamental frequency waveform.

The DC source for the first H-bridge ($H_1$) is a dc source with an output voltage of $V_{dc}$, whereas the dc source for the second H-bridge ($H_2$) is a DC source voltage to be held at $V_{dc}/2$. The output voltage of the first H-bridge is denote by $v_1$ and the output of the second

H-bridge is denote by $v_2$. Hence the output of this two dc sources cascaded H-bridge multilevel inverter is $v = v_1+v_2$. By opening and closing the switches of $H_1$ suitably, the output voltage $v_1$ can be made equal to $V_{dc}$, 0, or else $-V_{dc}$ when the output voltage of $H_2$ can be made equal to $V_{dc}/2$, 0, or else $-V_{dc}/2$ by opening and closing its switches suitably. Therefore, the output voltage of the inverter may have the values $V_{dc}$, $V_{dc}/2$, 0, $-V_{dc}/2$, and $-V_{dc}$ which are five levels. The output voltage of the cascaded multilevel inverter is

$$v = v_1 + v_2 \qquad (1)$$

*i) Harmonics*

The switching angles of the waveform will be adjusted to obtain the lowest output voltage THD. The harmonics orders and magnitude are depends up on the type of inverter and the control techniques. For example in single phase VSI, the output voltage waveform typically consists only of odd harmonics. The even harmonics are not present due to the half wave symmetry of the output voltage harmonics. The harmonic spectra depend on the switching frequency and the control method [6].

*ii) Switching control of the inverters*

There are number of modulation control techniques such as sinusoidal PWM method (SPWM) [7-11], space vector PWM method (SVPWM), selective harmonic elimination method (SHE) [12-14], and active harmonic elimination method [15], and they all can be used for inverter modulation control. For the proposed inverter control, a sensible modulation control method is the fundamental frequency switching control for high output voltage and Sinusoidal PWM control for low output voltage. In this paper, fundamental frequency switching control is used in H-bridge MLI [16].

## IV. SIMULATION OF FCMLI AND CASCADED H-BRIDGE MULTILEVEL INVERTER

The performance of the proposed Flying capacitor multilevel inverter is verified through the simulation results.

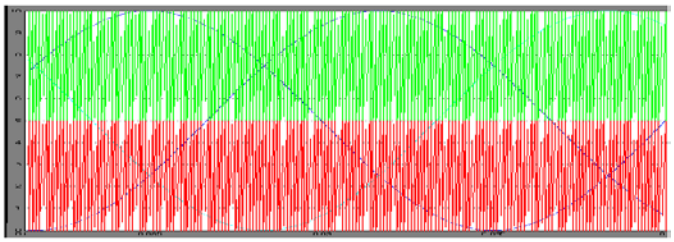

Fig. 4 Sinusoidal PWM signals for FCMLI.

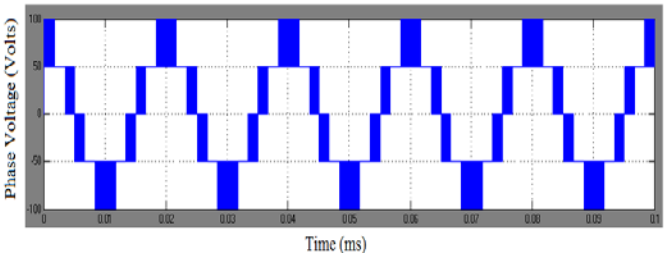


Fig. 5 Phase voltage of FCMLI.

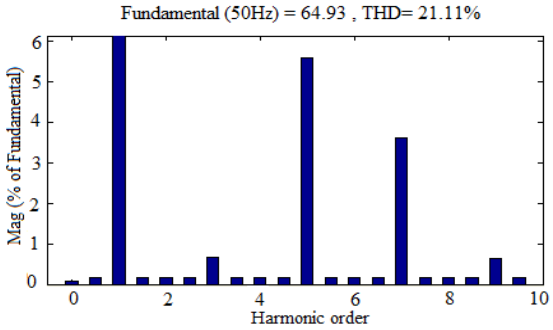


Fig. 6 FFT analysis of FCMLI voltage.

The Fig. 4 shows the sinusoidal PWM control for low output voltage. Fig. 5 and Fig. 6 show the FCMLI phase voltage, and FFT analysis of voltage respectively.

The performance of the proposed H-bridge multilevel inverter is verified through the simulation results. Fig. 7 shows the phase voltage of cascaded H-bridge multilevel inverter. Fig.8 shows the FFT analysis of voltage.

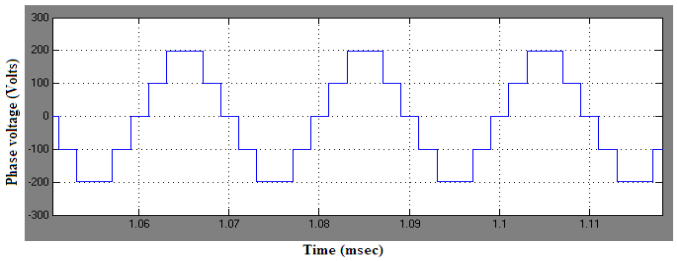


Fig. 7 Phase voltage of cascaded H-bridge multilevel inverter.

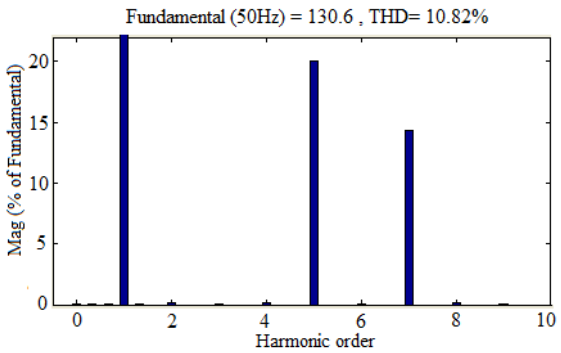


Fig. 8 FFT analysis of Cascaded H-Bridge MLI voltage.

TABLE II

PERFORMANCE PARAMETERS OF FIVE LEVEL FCMLI AND H-GRIDGE MULTILEVEL INVERTER

| Perameter | FCMLI | H-Bridge MLI |
|---|---|---|
| **THD %** | 21.11 % | 10.82 % |

Table II shows the THD performance of five level FCMLI and cascaded H-bridge multilevel inverter. Comparing both MLI cascaded H-bridge multilevel inverer gives the less value of THD (10.82%).

## V. VI. CONCLUSION

The flying capacitor multilevel inverter uses a ladder structure of dc side capacitors where the voltage on each capacitor differs from that of the next capacitor. The sinusoidal PWM scheme is used for modulation control. In cascaded H-bridge multilevel inverter separated unequal DC sources are used to generate sinusoidal output. A fundamental switching scheme is used and produces a nearly sinusoidal output. This cascaded inverter design is to get the improved sinusoidal output of an inverter and gives reduced THD%. The elimination of harmonics in a cascade H-bridge multilevel inverter by considers the inequality of separated dc source. FFT spectrum shows the reduction in the harmonics in the output voltage.

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