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SELF HEATING EFFECTS IN SOI TECHNOLOGY

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Abstract: For more than three decades, it has been searching for a way to enhance existing silicon technology to speed up the computer performance. The Silicon on Insulator (SOI) technology results in faster computer chips with low frequency noise that also require less power a key requirement for extending the battery life of small, hand-held devices that will be pervasive in the future. SOI is a major breakthrough because it advances chip manufacturing one to two years ahead of conventional bulk silicon. It provides a step-by-step look at the developments leading up to the development of SOI technology. Increased demand for High Performance, Low Power and Low Area among microelectronic devices is continuously pushing the fabrication process to go beyond ultra deep sub-micron (UDSM) technologies such as 45nm, 32nm and so on. Currently, chips are being designed in 55nm, 45nm and 32nm process nodes. The performance and power goals for certain applications in these advanced nodes couldn't be achieved with conventional silicon bulk Complementary Metal oxide semiconductor (CMOS) process leading to an alternative, Silicon on Insulator SOI process. Silicon on Insulator fabrication process helps in achieving greater performance and offers less power consumption compared to the Bulk Process.

Keywords: *Self-heating, impact ionization, kink effect, thermal conductivity, TCAD*

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1.1 Self Heating Effects in SOI Technology:

The presence of buried oxide could make the temperature of the channel rise more than in a classical transistor on Bulk, especially in the case of continuous current flow e.g. in analog biasing circuits is defined as self heating in SOI. Due to thermal isolation of substrate by the buried insulator in an SOI transistor, removal of excess heat generated by the Joule effect within the device is less efficient than in bulk, which leads to substantial elevation of device temperature. The excess heat mainly diffuses vertically through the buried oxide and laterally through the silicon island into the contacts and metallization. Due to the relatively low thermal conductivity of the buried oxide, the device heats up to 50ºC to 150ºC. This increase in device temperature leads to a reduction in mobility and current drive, thus degrading the device performance over a period of time.

1.2 Impact Ionization: If kink effect is attributed entirely to impact ionization effects then Ids= Idso +Ikink with Ikink = MIdso where Idso is the current that would be obtained if impact ionization effects were absent. When impact ionization is present, it provides a source of current and the electron current equation has the modified form impact ionization source is usually modeled by $GI-I = -\alpha nJn$ with $\alpha n = An \exp(-\beta n / F)$ with n α strongly dependent on the electric field strength F.

1.3 Floating Body and Parasitic Bipolar Effects

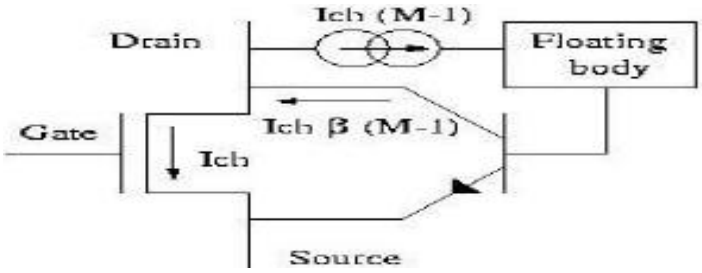

Figure 1.1 Parasitic bipolar transistor of the SOI MOSFET

The presence of a floating volume of silicon beneath the gate is at the origin of several effects unique to SOI, generically referred to as floating body effects. There exists a parasitic bipolar transistor in the MOS structure. If we consider an n-channel device, the N+ source, the P-type body and the N+ drain indeed form the emitter, the base, and the collector of an NPN bipolar transistor, respectively. In a bulk device, the base of the bipolar transistor is usually grounded by means of a substrate contact. But, due to the floating body in an SOI

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transistor, the base of the bipolar transistors is electrically floating. This parasitic bipolar transistor in figure 1.1 is origin of several undesirable effects in SOI devices.

1.4 Self Heating Effect

These effects arise in SOI devices because the device is thermally insulated from the substrate by the buried oxide BOX. Consequently, removal of excess heat generated within the device by device switching is not removed as efficiently in SOI devices as it is in bulk devices. This leads to a substantial elevation of temperature within the SOI device 50º-150ºC as shown in figure 1.2. This self-heating effect only appears when power is being dissipated within the device that is when the transistor is on, conducting current through its channel. This only occurs in CMOS circuits when a logic stage is switching state, not when it is in a stand-by state e.g., holding logic high or low state.

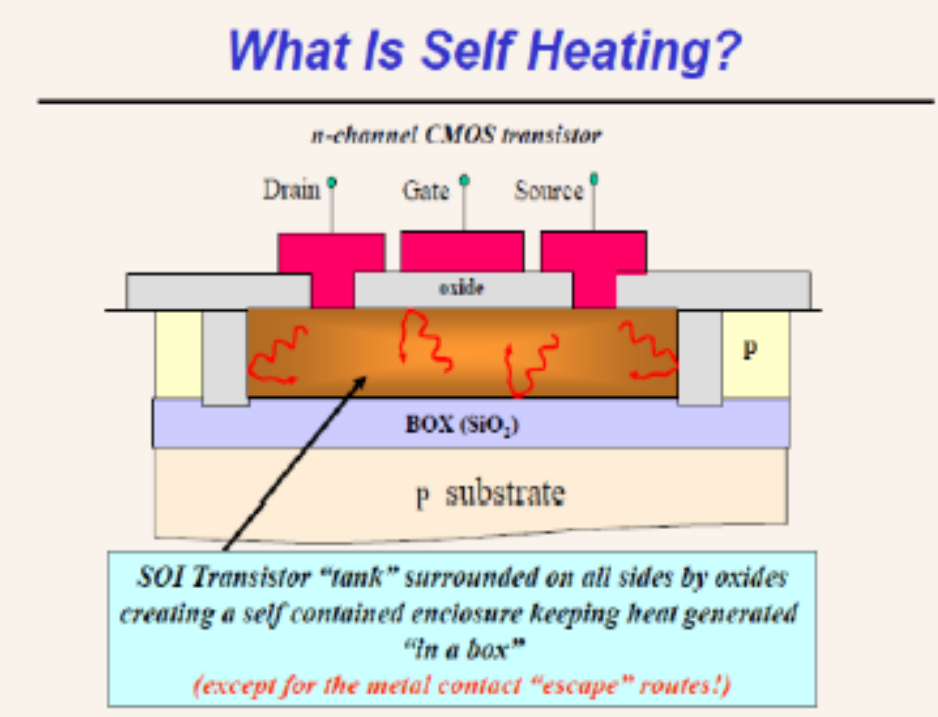

Figure 1.2 Self heating effects in SOI transistor

These effects certainly will not prevent the widespread adoption of SOI for CMOS ICs, but they must be taken into account by thoughtful device and circuit design approaches that specifically address the peculiarities of the SOI CMOS transistor vs. the bulk or epitaxial wafer CMOS transistor. Obviously, the process simulation, device simulation, circuit simulation, and layout Technology Computer Aided design (TCAD) tools employed by designers must accurately model the peculiarities and advantages of SOI CMOS to achieve optimal device design, circuit design, layout and processing approaches for CMOS ICs

fabricated with SOI wafers. CMOS transistors designed for use with SOI wafers are classified by the thickness of the device-quality single-crystal silicon layer at the surface above the BOX relative to the depths of the source-drain junction and channel depletion layers in the device with the operating voltages applied. An SOI CMOS transistor is classified as "partially depleted" (PD) if the silicon surface layer is thicker than the depth of the depletion region in the transistor's channel. The SOI CMOS transistor is classified as "fully depleted" (FD) if the silicon surface layer is equal to the depth of the depletion region in the transistor's channel.

The transistor will be partially depleted or fully depleted depending on the silicon layer thickness above the BOX and the doping concentration in the channel. To form a fully depleted SOI transistor, the channel doping concentration must be low enough the gate depletion region extends throughout the entire thickness of the silicon layer. When the silicon surface layer is thicker than about 200nm, the transistor will typically be partially depleted, unless the channel doping concentration is reduced to such low values that the threshold voltage is too low for practical CMOS applications less than 100mV. If the silicon layer thickness is reduced to about 100nm, the transistor will be fully depleted, even when the channel doping concentration is increased to produce threshold voltages of 300-400mV. If the silicon layer thickness is reduced further 70nm, the transistor will remain fully depleted even if the channel doping concentration is increased to produce even higher threshold voltages 700mV.

There are significant differences in partially depleted and fully depleted SOI CMOS transistors. For example, the threshold voltage of the fully depleted device is very sensitive to the silicon surface film thickness. This results in an addition source of manufacturing variance in the fabrication of FD SOI CMOS. Typically, this is in the order of 10mV in threshold voltage per nanometer of variation in the silicon film over the BOX. The fabrication of commercial CMOS on SOI typically employs partially depleted PD devices. However, careful device design and optimizing the channel implant process can reduce this sensitivity in FD devices. The variation of drain saturation current does not have the same sensitivity to film thickness as the threshold voltage in FD SOI CMOS. There are significant advantages for FD transistors over PD transistors, and the trend in SOI CMOS is toward the use of fully depleted devices. A fundamentally important point is that in FD SOI CMOS the

sub threshold slope can be very low less than ~65 mV/decade i.e., a 65 mV increase in gate voltage will result in a tenfold increase in the sub threshold drain current.

The differential equation describing heat transfer is:

$$\Delta T = \frac{c\rho}{\lambda}\frac{\partial T}{\partial t}$$

- λ: thermal conductivity, [W/m°C]
- c: specific heat, [J/kg°C]
- ρ: material density, [kg/m3]
- T: temperature, [°C]
- λ/cρ: thermal diffusivity, [m2/s]

These effects arise in SOI devices because the device is thermally insulated from the substrate by the buried oxide (BOX). Consequently, removal of excess heat generated within the device by device switching is not removed as efficiently in SOI devices as it is in bulk devices. This leads to a substantial elevation of temperature within the SOI device 50º-150ºC.

The insulation layer of the SOI wafer creates a potential temperature delta between devices called local (self) heating. Self-heating is evident at the high power regions. It May not have huge impact on Digital circuits; however this effect must be considered for analog type of circuits. As CMOS technology scales down to deep sub-micron dimensions, power density increases accordingly, thus resulting in remarkable temperature increases in the active devices. This problem has become even more critical with the introduction of SOI technologies, where the low thermal conductivity of the insulation layer below the top silicon film inhibits an efficient heat flow through the substrate as in standard bulk CMOS technologies. Semiconductor components are really sensitive to temperature variations. The impact of raised operating temperatures in both analog and digital circuits increases self heating effect. Self heating in SOI can cause device and interconnect temperatures to raise more than 10º-12ºC.

The self Heating effects can be summarized as follows:

- Degraded carrier mobility which leads to a reduced on-current of transistors and thus slower speed
- Higher interconnect metal resistivity which yields longer delays

- Increased failure rate
- Reduced reliability of electronic devices, with secondary effects such as interconnect electromigration

Self-heating phenomena are studied from room down to near liquid helium temperatures in fully depleted N channel thin film SIMOX MOS devices. A simple theoretical analysis of the self-heating effect is worked out. A method for the extraction of the thermal resistance and the device temperature rise directly from the static output characteristics is derived. Also direct self heating transient measurements are conducted.

SOI MOS devices are well known to suffer from self-heating phenomena arising from the low thermal conductivity of the buried oxide compared to Si substrate. At sufficiently high current levels, this result in the occurrence of negative output conductance in the saturation region. Self-heating effect is studied from room down to near liquid helium temperatures on fully depleted N channel thin film SIMOX MOS devices. Moreover, a simple self-heating model is proposed enabling the extraction of the thermal resistance and the average temperature rise of the device directly from the static output characteristics.

SOI devices suffer from the self-heating because of the existence of buried oxide BOX. Velocity overshoot should be considered to evaluate the self-heating effect in deep sub micrometer region. Drain current degradation due to the self heating effect in sub-0.1µm SOI MOSFETs is investigated, focussing on the comparison with bulk devices. It is revealed that the velocity overshoot can reduce the self-heating effect as well as the difference of the current degradation between SOI and bulk device.

In the bulk technologies, heat generated by charge transfer in the transistor is readily transferred out of the chip backside through silicon substrate. This transfer of heat is quick enough so that local device transconductance changes due to self-heating are negligible. For bulk devices with six or more layers of interconnect, the stacked inter-layer dielectrics ILDs present substantial thermal resistance. However, in the current generation of submicron technology bulk devices, these thermal issues are being addressed with the use of reduced dielectric constant dielectrics and higher conductivity metallization based on copper interconnect. In SOI technology, silicon dioxide comprises the BOX layer, so that the SOI transistor is encased in a perfect little insulated region of its own. As a result, the average junction temperature of SOI devices can be somewhat higher than for an identical bulk

device, reducing the device transconductance. Since SOI transistors are thermally insulated from the substrate by the buried insulator, the removal of excess hear generated by the Joule Effect, within the device is less efficient than in the bulk devices. The excess heat has several conduction paths, diffusing vertically through the buried oxide and laterally through the silicon island into the contacts and the metallization.

Thus, SOI MOSFETs are susceptible to the local thermal heating generated in the channel due to less thermal conductivity of the buried oxide, which is approximately 100 times lower than thermal conductivity of silicon. The self-heating causes a reduction of the carrier mobility, shifts the threshold voltage, and results in a negative differential conductance at high gate and drain voltages. The negative resistance, which can be seen in the output characteristics of SOI Metal oxide semiconductor Field Effect Transistors (MOSFETs) is due to a mobility reduction effect caused by device self heating. This effect can compromise reliability of the part when the part is operating at low and ultra low temperatures due to thermo-mechanical stresses and possible formation of structural defects and microcracks.

CONCLUSION:

In SOI devices, self-heating effect can be minimized by using a thin buried oxide film; thus, decreasing the bottom layer thermal resistance. Another advantage of this approach is the reduction of short channel effect for the back transistor. However, the back channel transistor threshold voltage is reduced if the doping level at the back channel interface is not increased. This, in combination with a floating body effect, can lead to a worst case behaviour. The self-heating effect is more pronounced in fully-depleted structures due to thinner silicon films, which means a thinner buried oxide will be required to minimize it. The limitation for thinning the buried oxide is imposed by the variations of the threshold voltage with the backgate bias. Fully depleted devices exhibit a different electrical behaviour from the partially depleted devices. The threshold voltage varies with the backgate bias for enhancement mode and accumulation mode devices due to the coupling effect between the front and the back gates when the silicon film is fully depleted. As a result of this coupling effect, the threshold voltage of fully depleted devices becomes a function of the silicon and buried oxide thicknesses.

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REFERENCES:

[1] L.T. Su, et al., IEEE trans. Electron Devices, Vol. 41, no.1, p 69, Jan. 1994.

[2] J. B. Roldan, et al., IEEE Electron Device Lett., vol. 21, no.5, May 2000.

[3] H. Kawashima and R. Dang, IEICE Trans. Electron. Vol. E82-C, p.894, 1999.

[4] K. Matsuzawa, I. Kamohara and T. Wada, in NASECODE VII, P.173, 1991.

[5] J. Jomaah, F. Balestra, and G. Ghibaudo, " Self-heating effect in SOI MOSFETs operated at low temperature," in SOI Conf. Dig., 1993, pp. 82-83.